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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Katsumi MIYATA et al.

Serial Number: **09/478,508**

Group Art Unit: **2814**

Filed: **January 6, 2000**

Examiner: **GRAYBILL, D.**

For: **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Date: October 18, 2001

Sir:

In response to the Office Action dated June 19, 2001, please amend the above identified application as follows:

IN THE CLAIMS:

Please **CANCEL** claim 13.

Please **AMEND** claims 16 and 17 as follows:

16. (Amended) A semiconductor device having a semiconductor chip,

first electrodes formed on said semiconductor chip,

barrier metals formed on said first electrodes and having laminated structures, and

a plurality of second protruded electrodes, which serve as external connection terminals, formed on said barrier metals, wherein said barrier metals comprising:

a lowermost conductive metal layer laminated on said first electrodes, said lowermost conductive metal layer having a joining property with said first electrodes;

an intermediate conductive metal layer laminated on said lowermost conductive metal layer, said intermediate conductive metal layer comprising one or more layers and having a joining property with said lowermost conductive metal layer, said intermediate conductive metal layer having at least one layer serving as a barrier layer for preventing said protruded electrodes from diffusing into said intermediate conductive metal layer; and

an uppermost conductive metal layer laminated on said one or more intermediate conductive metal layers, said uppermost conductive metal layer being made of a material which easily alloys with the material of said intermediate conductive metal layers and which has resistance to oxidation,

wherein said uppermost conductive metal layer is made of a metal selected from the group consisting of gold (Au), platinum (Pt), palladium (Pd), silver (Ag) and rhodium (Rh) or of an alloy containing a metal selected from the group consisting of gold (Au), platinum (Pt), palladium (Pd), silver (Ag) and rhodium (Rh).

17. (Amended) A semiconductor device as claimed in claim 16, wherein the weight of said uppermost conductive metal layer is less than 2 weight % of the weight of the bump to be formed thereon.

REMARKS

Claims 16 and 17 are pending in this application. Claim 13 has been canceled here. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made."

Rejections under 35 USC §112, Second Paragraph

Claims 13, 16 and 17 were rejected under 35 USC §112, second paragraph, as being indefinite because, in claim 13, the term "good" is a vague relative term of degree for which the disclosure provides no clear standard for measuring the degree, or it is not apparent if the degree is limited by the disclosure, and one of ordinary skill in the art in view of the prior art and the status of the art would not otherwise be reasonably apprised of the scope of the term.

In order to overcome the rejection, "comparatively good" has been deleted from the claims.

Rejections under 35 USC §102(b)

Claims 13 and 16 are rejected under 35 USC §102(b) as being anticipated by Cook (U.S. Patent No. 5,719,070).

Claim 16 has been amended to recite the materials forming the barrier metal. Amended claim 16 patentability distinguishes over Cook.

Cook merely discloses a normal barrier metal known in the art. In Cook, the barrier metal serves to improve a joining property against solder and to prevent the solder from being diffused. The barrier metal is formed and then the solder bump is formed. Then, a probe test is performed by contacting a probe with the solder bump. However, Cook does not teach that the probe test is performed on the barrier metal.

If a normal barrier metal such as the one known from Cook is used for a method in which a probe test is performed before forming the solder bump, the barrier metal will be oxidized during the probe test. This should be avoided because it is difficult to form the solder bump on the oxidized barrier metal.

Claim 16 recites that the "uppermost conductive metal layer is made of a metal selected from the group consisting of gold (Au), platinum (Pt), palladium (Pd), silver (Ag) and rhodium (Rh) or of an alloy containing a metal selected from the group consisting of gold (Au), platinum (Pt), palladium (Pd), silver (Ag) and rhodium (Rh)." Such a combination of materials provides a resistance to oxidation. With such a barrier metal, a probe test can be directly performed on the barrier metal, since the barrier metal will not be oxidized during the probe test. Cook does not teach or suggest such features as recited in claim 16.

For at least these reasons, claim 16 patentably distinguishes over Cook. Claim 17, depending from claim 16, also patentably distinguishes over Cook for at least the same reasons.

It is submitted that nothing in the cited references, taken either alone or in combination, teaches or suggests all the features recited in each claim of the present invention. Thus all pending

claims are in condition for allowance. Reconsideration of the rejections, withdrawal of the rejections and an early issue of a Notice of Allowance are earnestly solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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